Digital ASIC Fabrication

or

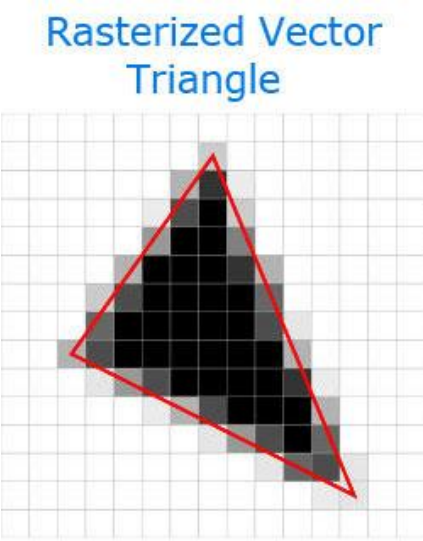
µGPU

sdmay26-24

Team Members

- Colin McGann (Project Lead)
- Dawud Benedict (Toolflow)
- Michael Drobot (Firmware)
- Jack Tonn (Testbench and Validation)
- Samual Forde (PCB and Layout)
- Emil Kosic (Repo and Coding Standards)
- Joshua Arceo (Client/Advisor Communications)

Design Overview

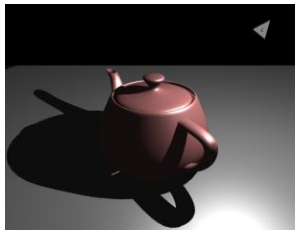


- Design a digital ASIC for fabrication, using the ChipForge toolchain
- Our project: A programmable 3D raster GPU
  - Output resolution: 320x240
  - Frame rate: 15Hz (minimum)
  - Output type: VGA
  - Programmability means we support other GPU tasks:
    ray tracing, ML, GPU compute, etc
- Our users: ChipForge members, ISU faculty, embedded GPU users
- Effective budget of only $45,000

Functionality

- Our GPU will be a low power alternative to modern GPUs
- Our GPU must be modifiable
  - Configurable Resolution & Refresh Rate
  - Must feature debug registers in critical sections
  - Must be able to take commands from an outside source
- The GPU will well documented, with a datasheet and a user guide
  - C code drivers will be included, along with an example project drawing triangles to the screen.

Inputs and Outputs



Model

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Vertices and Connectivity

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Vertex Shader Program

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Rasterizer

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Fragment Shader Program

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VGA Output

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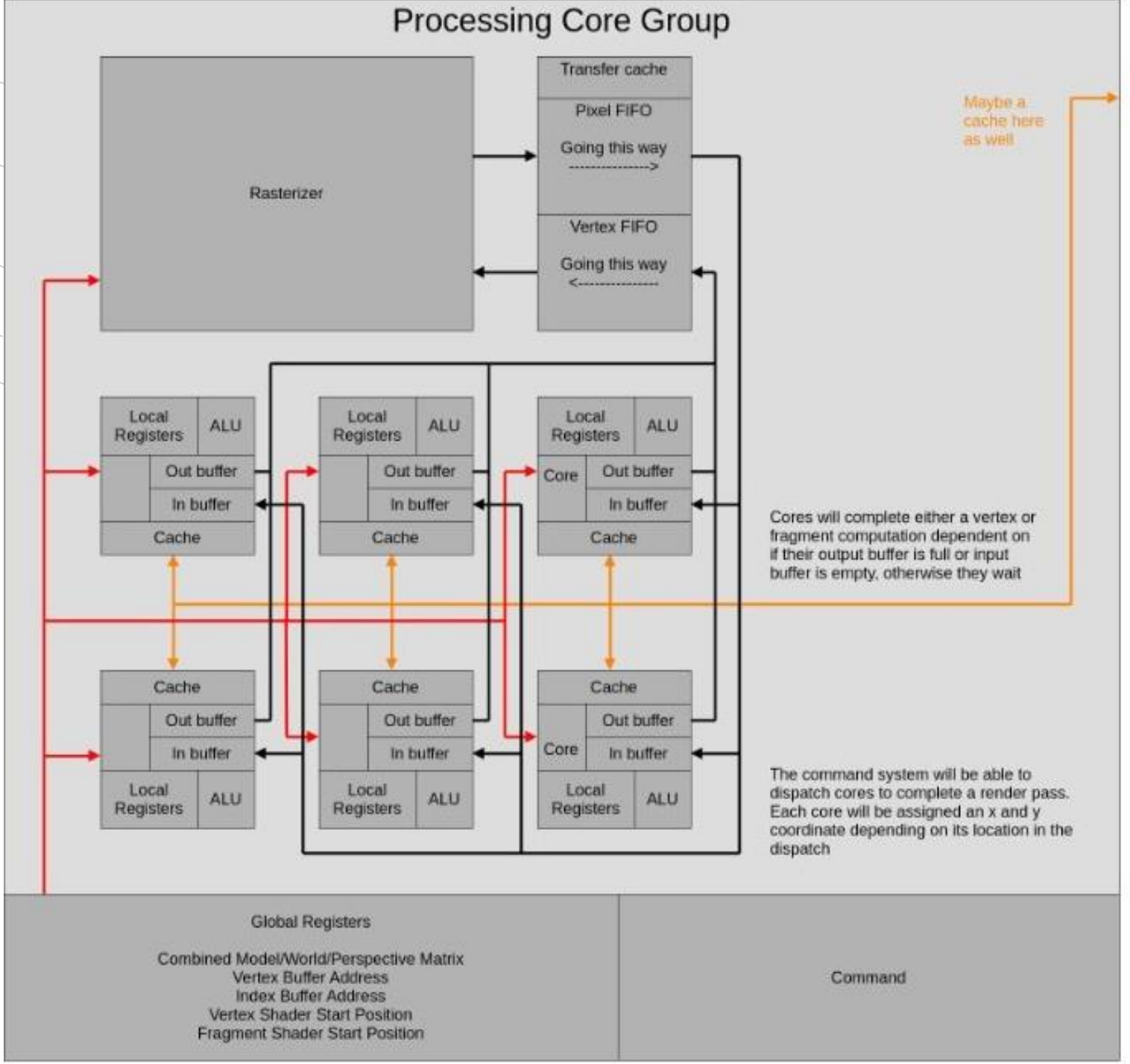
Screen

Placing objects in the world and projecting them onto the screen

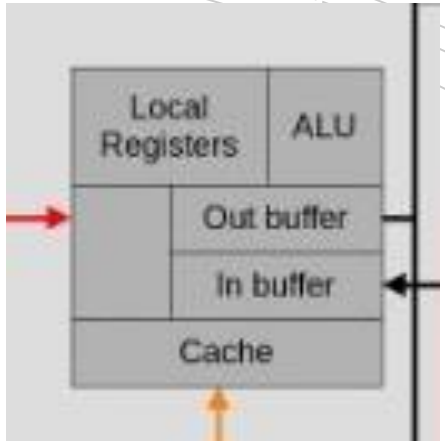
Checking visibility, applying textures

Lighting, smoothing, writing the frame

Detailed Design



Cores and ISA



- The cores run small assembly programs called shaders, using our custom ISA
  - Vertex shader: Placing objects in the scene and projecting them into the screen
  - Fragment shader: Applying lighting
- An ISA (instruction set architecture) is a set of basic operations allowed and implemented in hardware
- Support basic operations like add, sub, addi, subi, mult, dot product
- Instructions can access local registers (per core) and global registers (shared to all cores)
- Instruction and word size of 32 bits

Areas of Concern and Development

- We only have 10 square millimeters of area
- We have very few opportunities to silicon-prove our designs
  - The chips we get back may not work at full speed or have hardware issues
- There is a strict tapeout submission deadline
- The fabrication company could shut down

Questions?